MICROCOMPUTER TECHNOLOGY PROJECTIONS

I. Microcomputer/microprocessor parts

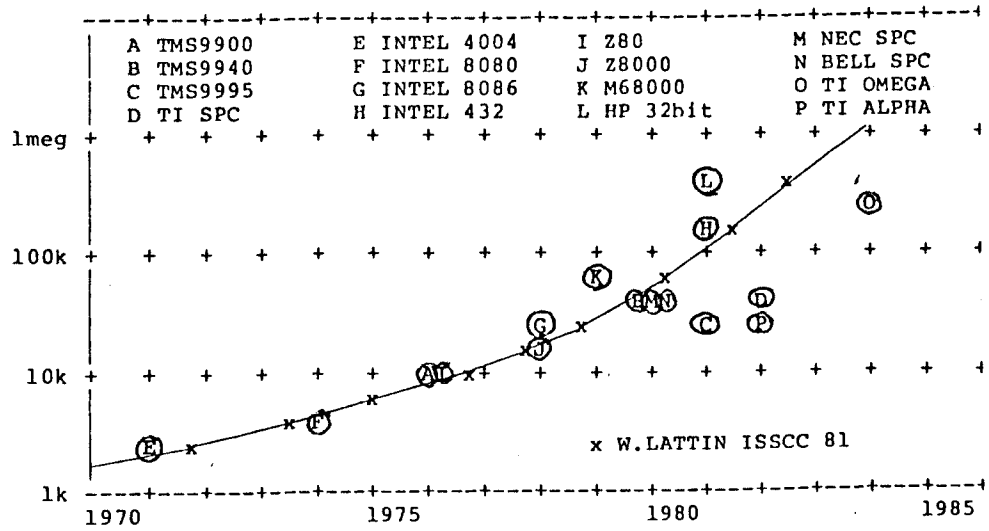
ID	Word (bits)	Xsistrs	Tech.	ROM (bits)	RAM (bits)	MIPS	Area (mm^2)	Power (Watts)	Rules (um)	Year
I 4004	4	2300	PMOS			0.1				1971
I 8080	8	4500	NMOS		124	0.5	22	1.2		1974
I 8086	16	29000	NMOS			2.5				1978
I 432	32	110000	NMOS	64000		10.0	66	2.0	4.0	198?
I 2920	25		NMOS	4608	1000	2.5	30			1979
Z-80	8	8200	NMOS		124	1.0	27	1.0		1976
Z-8000	16	17500	NMOS		272	1.3	39	1.5		1977
M-6800	8		NMOS			1.0				1975
M-68000	16	68000	NMOS		512	2.0	45	1.2	3.2	1979
TMS-1000	4		PMOS	8192	256	0.16				
TMS-9900	16	8300	NMOS	0	0	0.5	37	0.25	5.0	1976
TMS-9940	16	37000	NMOS	16000	1024	0.6	30		4.5	1980
TMS-9995	16	29000	NMOS	0	2048	0.75	29		4.5	198?
TMS-7020	8		NMOS	16000	1024	1.25			4.5	1981
TI SPC	16	38600	NMOS	24576	2304	5.0	35	1.0	3.0	1982
HP	16	9600	CSOS		128	0.95	34	0.5	6.0	197?
RCA	8	5500	CMOS			0.40	26			1977
INTEL	8		NMOS		512	0.40				1977
NEC	16	15000	CMOS			0.63	33			197?
Fujitsu	16	40000	CMOS		512	2.5	111	0.13		1978
NEC SPC	16	40000	NMOS	18400	2048	4.0	28	0.9	3.0	1980
BELL SPC	20	45000	NMOS	16384	5120	5.0	69	1.5		198?
HP	32	450000	NMOS		960	18.0	40	7.0	1.25	1981
DEC 11/23	16	17000	NMOS	12000		7.5	25	0.8	5.0	1981
Toshiba	16	48000	CSOS		528	3.3	50	0.6	5.0	198?
BELL	32	100000	CMOS		544	16.0		1.2	3.5	1981

* These figures are based on incomplete information. I would appreciate any corrected data (R.Pettengill, 995-7908, MSG ULSI).

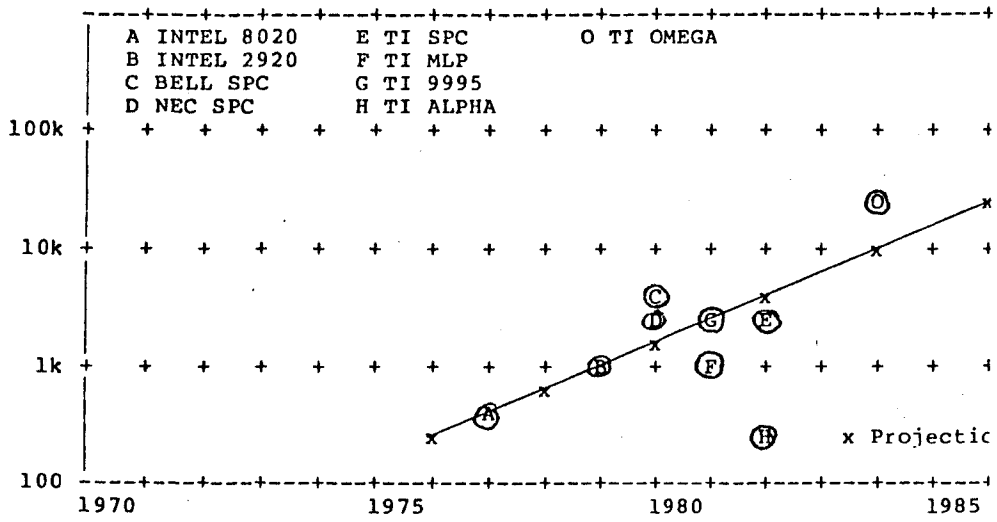
Moore Business Forms, Inc.

MICROCOMPUTER TECHNOLOGY PROJECTIONS

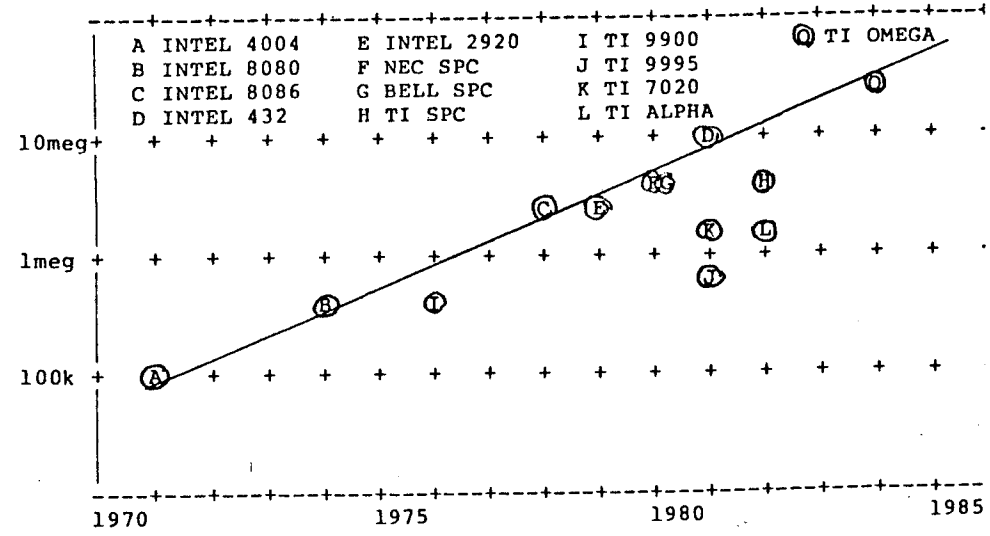
TOTAL NUMBER OF TRANSISTORS (INCLUDES ALL ROM BITS)



MICROCOMPUTER ON CHIP RAM (bits)



MICROCOMPUTER SPEED (microinstructions per second)



RCP 2-28-81

MICROCOMPUTER TECHNOLOGY PROJECTIONS

SPC - 68K

I. Microcomputer/microprocessor parts

ID	Word (bits)	Xsistrs	Tech.	ROM (bits)	RAM (bits)	MIPS	Area (mm^2)	Power (Watts)	Rules (um)	Year	Source	Multip Accum μ.sec
I 4004	4	2300	PMOS			0.1				1971		
I 8080	8	4500	NMOS		124	0.5 1.25	22	1.2		1974		
I 8086-5Mhz	16	29000	NMOS			~~2.5*~~	32	1.5	4.0	1978		25.7
I 432	32	110000	NMOS	64000	.5	10.0	66	2.0	4.0	1981	81 isscc	
I 2920	25		NMOS	4608	1000	2.5	30			1979	79 ISSCC	2μ
Z-80	8	8200	NMOS		124	1.0	27	1.0		1976		
Z-8000-4Mhz	16	17500	NMOS		272	1.3	39	1.5		1978		
M-6800	8		NMOS			1.0				1975		
M-68000-4Mhz	16	68000	NMOS		512	2.0	45	1.2	3.2	1979		18.0
TMS-1000	4		PMOS	8192	256	0.16						
TMS-9900-3Mhz	16	8300	NMOS	9000	0	0.2	37	0.25	5.0	1976		
TMS-9940-4Mhz	16	37000	NMOS	16000	1024	0.25	30		4.5	1980		
TMS-9995-3Mhz	16	29000	NMOS	4500	2048	~~0.75~~ 1.0	~~29~~ 40	.7	4.5	1981		9.0 ~~1.8~~
TMS-7020-5Mhz	8		NMOS	16000	1024	~~1.25~~ .5	23	.4	4.5	1981		19.2 ~~[illegible]~~
TI SPC-5MHz	16	38600	NMOS	24576	2304	5.0	~~28~~ 44	1.0	3.0	1982		0.4
HP	16	9600	CSOS		128	0.95	34	0.5	6.0	1977	77 ISSCC	
RCA	8	5500	CMOS			0.40	26			1977	77 ISSCC	
INTEL	8		NMOS		512	0.40				1977	77 ISSCC	
NEC	16	15000	CMOS			0.63	33			1978	78 ISSCC	
Fujitsu	16	40000	CMOS		512	2.5	111	0.13		1978	80 ISSCC	
NEC SPC	16	40000	NMOS	18400	2048	4.0	28	0.9	3.0	1980	80 ISSCC	0.9
BELL SPC	20	45000	NMOS	16384	5120	5.0	69	1.5		1980	80 ISSCC	0.5
HP	32	450000	NMOS	342000	960	18.0	40	7.0	1.25	1981	81 ISSCC	
DEC 11/23	16	17000	NMOS	12000		7.5	25	0.8	5.0	1981	81 ISSCC	
Toshiba	16	48000	CSOS		528	3.3	50	0.6	5.0	1981	81 ISSCC	
BELL	32	100000	CMOS		544	16.0		1.2	3.5	1981	81 ISSCC	
OMEGA	24	250000	CMOS		24000	30.0			1.5			0.58
RIC	32	500000	CMOS		64000	30.0			1.5			4.5
ALPHA-24Mhz	16	34000	NMOS	20000	256	2.0	33	.8	3.0	1981		
~~SPC~~ -30Mhz												
MEP 4K												

* These figures are based on incomplete information. I would appreciate any corrected data (R. Pettengill, 995-7908, MSG ULSI).

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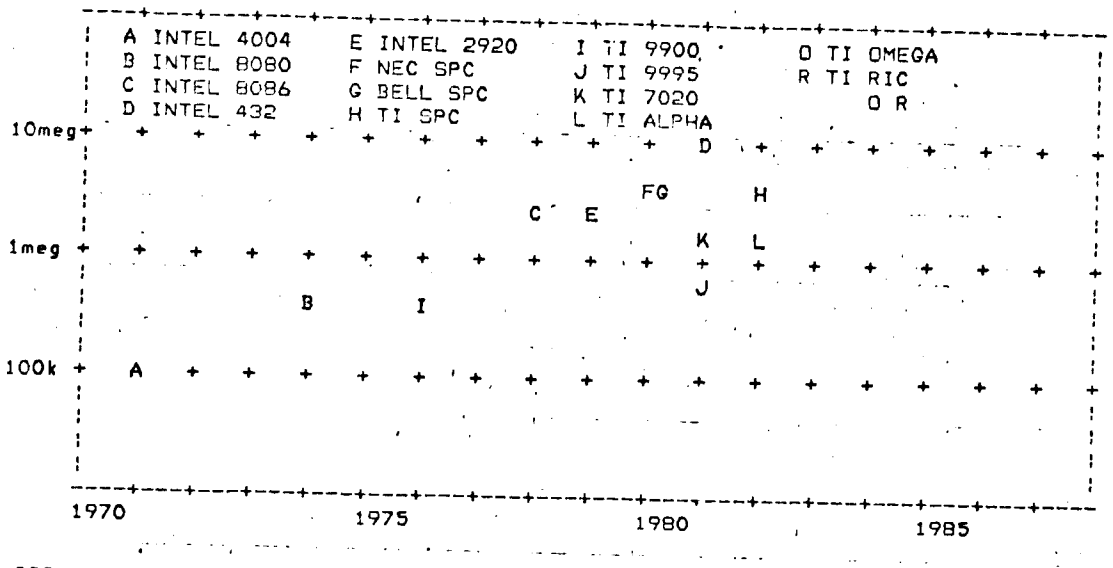
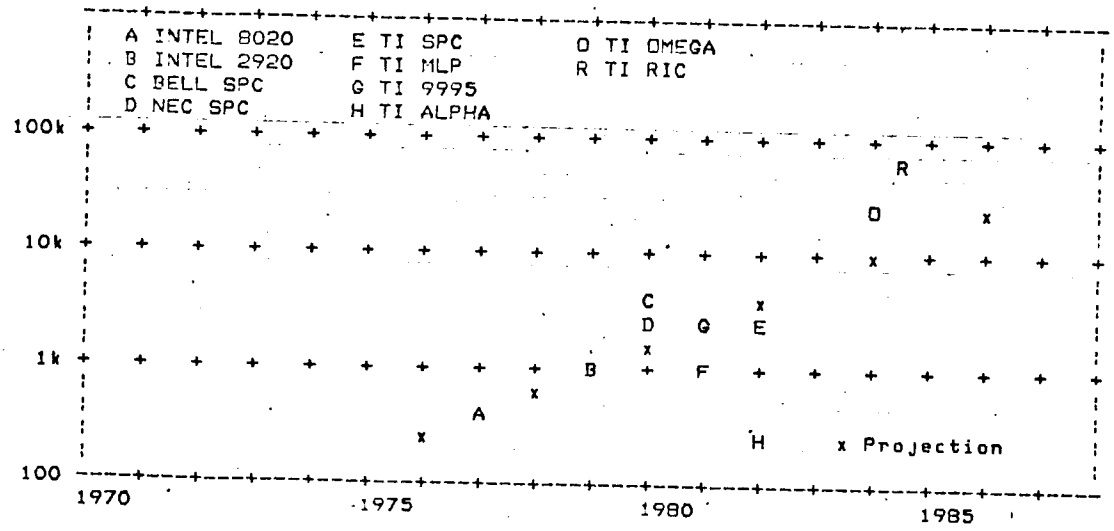
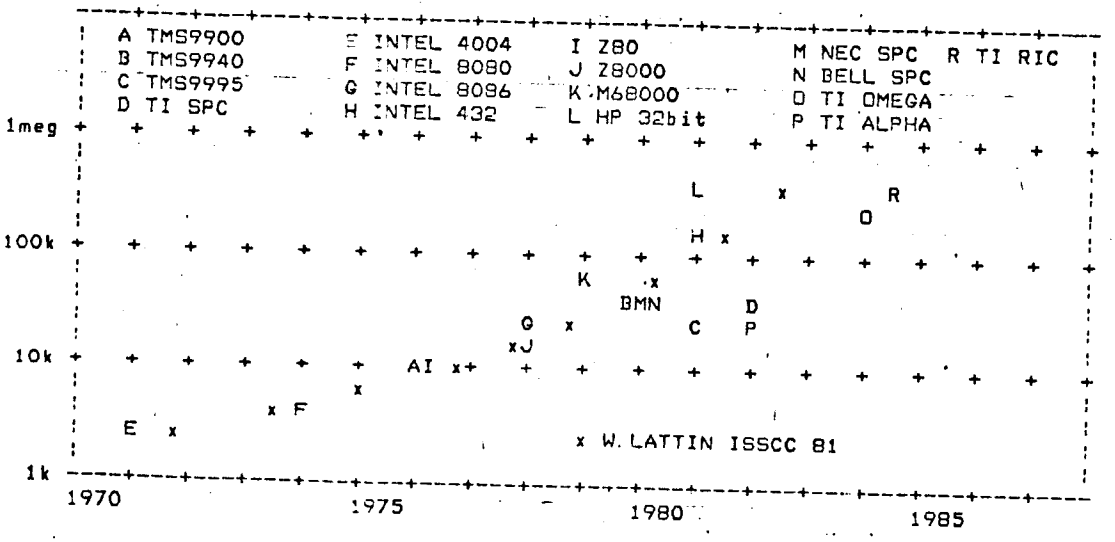
IV. MICROCOMPUTER SPEED (microinstructions per second)



III. MICROCOMPUTER ON CHIP RAM (bits)



II. TOTAL NUMBER OF TRANSISTORS (INCLUDES ALL ROM BITS)



MOS MICROCOMPUTER DESIGN
DEVICE COMPLEXITY

DEVICE	NUMBER OF TRANSISTORS			REGULARITY	
	RANDOM	DRAWN	TOTAL	% RAND	% TOT
5501	3400	856	3400	25.2	25.2
99000	11296	5799	71492	51.3	8.4
9918	8762	3717	9473	42.4	39.2
9900	8216	4320	16659	52.5	26.0
SPC	13079*	3815	55935	50.2	6.8
9995	9281	5043	35697	54.3	14.1
MPIF	3696	1242	16124	33.6	7.7
9995SE	9146	4900	22077	53.5	22.2
9909	8759	4323	22271	49.4	19.4
9914	3800	2385	3550	62.8	67.2
2220	5519	1647	24918	29.8	6.6
7020	5245	2682	36551	51.1	7.3
7040	5254	2682	53479	51.0	5.0
70L22	5087	2825	35250	55.5	8.0
70E40	5475	2900	58028	52.3	5.0

* 5483 MULTIPLIER

N-CHANNEL SI-GATE
DESIGN PARAMETERS

1st P.G. DATE	DEVICE	AREA	ROM BITS	RAM BITS	NO. TRANS.	AREA TRAN	MM ENG	MM DRAFT	COST $K
10/74	5501	42K			3.4K	12.3	24	17	200
1/75	8080	48K			4.8K	10.0	41	35	600
10/75	9900	58K	8K		8.3K	6.5	85	62	620
12/75	5502	39K	1.3K		5.8K	7.0	20	10	179
3/76	8080A	41K			4.8K	8.5			
10/76	9901	18K			2.6K	6.9	10	8	89
10/76	9902	15K			3.3K	4.6	23	10	204
4/77	9971	38K			6.6K	5.8	50	32	351
5/77	9972	40K	15K	1K			8	6	102
6/77	5513	29K			3.5K	8.3	15	12	83
9/77	9912	56K			4.1K	12.6	54	17	400
11/77	9903	46K	3.1K		6.9K	6.3	26	58	357
1/78	9940M	76K	20K	0.3K	8.3K	6.3	109	96	800
6/78	9918	62K			8.7K	7.1	59	39	387
10/79	9909	50K	10K		8.6K	5.5	56	71	521
9/80	9995	63K	5K	2K	9.3K	5.7	110	60	867
10/80	MLP	35K	23K	1K	5.2K	4.1	56	40	681
7/81	ALPHA	52K	22K	.3K	10.5K	4.3	149	121	1900
8/81	MPIF				1.7K		17	11	
10/81	SPC	67K	24K	2.3K	13.4K	3.6	89	41	823

* SHRINK