3.6 TMS 9985 INSTRUCTION EXECUTION TIMES

Instruction execution times for the TMS 9985 are a function of:

1. Clock Cycle time $t_c(\emptyset) = 2 \cdot t_{cy}$
2. Addressing modes used where operands have multiple addressing mode capability
3. Number of wait states required per external memory access

Table 5 lists the number of clock cycles and memory accesses required to execute each TMS 9985 instruction assuming that all memory accesses (including the instruction fetch) are to the internal RAM. The TMS 9985 will automatically add 1 wait state to each external memory access, and additional wait states can be added as necessary using the READY input. For instructions with multiple addressing modes for either or both operands, Table 5A lists the number of clock cycles and memory accesses with all operands addressed in the workspace register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced table. The total instruction execution time for an instruction is:

$$T = t_c(\emptyset) \cdot (C + W \cdot Me)$$

Where:

T=total instruction time;
$t_c(\emptyset)$ = clock cycle time;

C = number of clock cycles for instruction execution plus address modification;

Me = number of external memory accesses.

As an example, the insruction MOV B is used in a system with $t_c(\emptyset)$ = 500NS. If all memory accesses (including the instruction fetch) are to the internal RAM and both operands are addressed in the workspace register mode.

$$T = .5(6+0) = 3.0\mu s$$

If the instruction fetch were to external memory, no additional wait states were required, and both operands were in internal RAM and addressed in the workspace register mode:

$$T = .5(6+1\cdot 2) = 4\cdot 0\mu s$$

If the instruction fetch were to external memory and both operands were addressed in the indirect mode in external memory (no additional wait states required) from internal workspace registers:

$$T = .5(8+1.4) = 6.0\mu s$$

INSTRUCTION	CLOCK CYCLES	MEMORY ACCESS	ADDRESS MODIFICATION
A	10	8	SEE TABLE 5A
AB	7	5	SEE TABLE 5A
ABS (MSB=0)	12	4	SEE TABLE 5A
(MSB=1)	12	6	SEE TABLE 5A
AI	12	8	
ANDI	12	8	
B	8	4	SEE TABLE 5A
BL	10	6	SEE TABLE 5A
BLWP	20	14	SEE TABLE 5A
C	10	6	SEE TABLE 5A
CB	7	4	SEE TABLE 5A
CI	12	6	
CLR	8	6	SEE TABLE 5A
COC	10	6	SEE TABLE 5A
CZC	10	6	SEE TABLE 5A
DCA	7	4	SEE TABLE 5A
DCS	7	4	SEE TABLE 5A
DEC	8	6	SEE TABLE 5A
DECT	8	6	SEE TABLE 5A
DIV (ST4 IS SET)	26	14	SEE TABLE 5A
(ST4 IS RESET)*	126	16	SEE TABLE 5A
IDLE	10	4	
INC	8	6	SEE TABLE 5A
INCT	8	6	SEE TABLE 5A
INV	8	6	SEE TABLE 5A
JUMP	6	2	
LDCR (C=0)	42	6	SEE TABLE 5A
(1≤C≤8)	8+2C	5	SEE TABLE 5A
9≤C≤15)	10+2C	6	SEE TABLE 5A
LI	12	8	
LIIM	10	4	
LIMI	14	6	
LWPI	12	6	

INSTRUCTION	CLOCK CYCLES	MEMORY ACCESS	ADDRESS MODIFICATION
MOV	8	6	SEE TABLE 5A
MOV B	6	4	SEE TABLE 5A
MPY	82	10	SEE TABLE 5A
NEG	10	6	SEE TABLE 5A
ORI	12	8	
RTWP	14	10	SEE TABLE 5A
S	10	8	SEE TABLE 5A
SB	7	5	SEE TABLE 5A
SBO	10	4	
SBZ	10	4	
SET 0	8	6	SEE TABLE 5A
SHIFT(C≠0)	12+2C	8	
(c=0, BITS 12-15) OF WRO = 0)	46	8	
(C=0, BITS 12-15 OF WRO=N≠0)	14+2C	8	
SOC	10	8	SEE TABLE 5A
SOCB	7	5	SEE TABLE 5A
STCR(c=0)	46	8	SEE TABLE 5A
(1≤C=8)	29	7	SEE TABLE 5A
(9≤C≤15)	46	8	SEE TABLE 5A
STST	8	6	
STWP	8	6	
SWPB	8	6	SEE TABLE 5A
SZC	10	8	SEE TABLE 5A
SZCB	7	5	SEE TABLE 5A
TB	10	4	
X**	6	4	SEE TABLE 5A
XOP	26	16	SEE TABLE 5A
SOR	10	8	SEE TABLE 5A
RESET FUNCTION***	16	10	

INSTRUCTION	CLOCK CYCLES	MEMORY ACCESS	ADDRESS MODIFICATION
INTERRUPT*** CONTEXT SWITCH	16	10	
LOAD FUNCTION***	16	10	

* EXECUTION TIME IS DEPENDENT ON THE PARTIAL QUOTIENT AFTER EACH CLOCK CYCLE DURING EXECUTION.

** EXECUTION TIME IS ADDED TO THE EXECUTION TIME OF THE INSTRUCTION LOCATED AT THE SOURCE ADDRESS.

*** RESET, LOAD, AND INTERRUPT VECTORS ARE LOCATED IN EXTERNAL MEMORY THUS THE MINIMUM EXECUTION IS 20 CLOCK CYCLES ASSUMING NO ADDITIONAL WAIT STATES AND ALL STORES ARE TO INTERNAL MEMORY.

TABLE 5A
ADDRESS MODIFICATION

ADDRESSING MODE	CLOCK CYCLES (C)
WR(T_s or T_d = 00)	0
WR indirect (T_s or T_d = 01)	2
WR indirect auto increment (T_s or T_d = 11)	4
Symbolic (T_s or T_d = 10, S or D = 0)	6
Indexed (T_s or T_d = 10, S or D ≠ 0)	8