Memo
from
MIKE BUNYARD

7/7/81

Jerry -

Please note that this applies to our current product — not the new one. I thought you might want some feedback.

Mike

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TEXAS INSTRUMENTS
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M E M O R A N D U M

July 7, 1981

TO: Don Bynum
Alan Lawson

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COPY TO: [redacted]

FROM: Mike Bunyard

SUBJECT: THE 99/4(A) AND THE TMS9995

After spending some time thinking how to use the TMS9995 in the 99/4B, I have drawn some conclusions with respect to the present 99/4(A) that I feel should be documented for future reference. These conclusions revolve around the fact that the TMS9995 does not duplicate the timing of the TMS9900, and are listed as follows.

Please note that I forsee no problems in the 99/4B, as we have the chance to design around the points in question.

Basic Timing

For a 12 MHz clock the TMS9900 has a state (cycle) time of 2/3us while the TMS9995 has one of 1/3us (which is one of the ways that it gains a considerable speed advantage over the TMS9900), but two 1/3us cycles for either memory or CRU are NOT equivalent to one 2/3us TMS9900 state time. The TMS9900 has a 500ns memory access while the TMS9995 has only a 448 ns memory access due to increased setup times and something else I don't know about. There is no margin in this for 450ns ROMs; thus, faster memories are required.

In Addition, the following items were noted.

* The TMS9995 signal CLKOUT takes the place of PH3* of the TMS9900, and it is twice as wide as PH3*. Many peripherals use both the leading and trailing edge of PH3* for timing, and the additional pulse width leaves less timing margin.

* The control signal DBIN* of the TMS9995 is not timed identical to the DBIN of the TMS9900; DBIN* is now a function of CLKOUT, and becomes valid 167ns later than that for the TMS9900. This implies that there will be a

data bus conflict for this period for our peripherals during which abnormally high supply currents will result.

* Additional logic will be necessary to separate WE* and CRUCLK* with MEMEN* being the separating variable. While this logic is of the inexpensive variety, it still takes up PCB real estate, requires some supply power, and worse yet, adds propogation delay to these signals. The same thing is true for IAQ and HOLDA with HOLD* being the separating variable, but there is uncertainty in doing this. It depends upon when HOLD* is applied. This one is not a worry on the 99/4(A), though.

maybe ok

* CRUCLK goes from 83 1/3ns on the TMS9900 to 167ns on the TMS9995. This should present no problem on the 99/4(A) as I see it at this time.

Use of the TMS9995 Internal RAM

The TMS9995 internal RAM is located in the address space our Memory Expansion responds to, and when the TMS9995 accesses its internal RAM, external memory control signals are asserted. The MEU will respond, but will become very sick when the memory cycle is aborted at the end of 1/3us rather than 2/3us later as the MEU expects it to. This is the real KILLER in that existing product is already in the field that expects 1us memory cycles. We can provide the extra logic required to trap these addresses in the MEU, but again this is not especially simple (or pleasing for that matter).

The TMS9995 memory map has its Timer memory mapped in this manner, and of course it is disjoint from the internal RAM. Trapping all of this out is not my idea of fun when there are cost constraints involved. Even as argumentative as Acker is, he would say ugly things about having to arrange his code around these disjoint memory areas.

I, for the moment, think that the method of refreshing the present MEU would present conflicts with the TMS9995 accessing due to its 1/3us state times. It can get back to the MEU 1/3us earlier than the TMS9900 can.

CRU Operation

With the exception of the previously mentioned 448ns CRU access, I don't see any problems in this area as the 99/4(A) doesn't decode CRUCLK as a function of the instructions involved....it simply uses only CRU types of instructions.

Miscellaneous

The TMS9995 gets its MSBY of a word transfer first and the LSBY second. The 99/4(A) does the reverse which allows a settling time for DBIN and A14 as they are used in the VDP, sound chip, and GROMs before allowing the respective chip selects to go true. Extra logic will be required to prevent high speed accesses of these devices. This again amounts to dollars, space, and power.

Mike Bunyard